A High Power DPDT MMIC Switch for Broadband Wireless Applications

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Abstract **– A new type of dual-pole double-throw (DPDT) antenna switch IC for broadband wireless applications has been developed. The IC exhibits a low insertion loss of 0.9 dB up to 5.0 GHz and 1.1 dB at 6 GHz, high power handling with P1dB about 34.5 dBm with a control voltage of 0/3 V and high linearity with input IP3 about 53 dBm.**

I. INTRODUCTION

As demand grows worldwide for dual-band, triple-band and 3G wideband CDMA handsets, broadband access markets in the area of wireless Internet and in-home multimedia distribution are being emerged. These applications will be implemented through the 802.11a system operating in the 5-6 GHz band. Therefore, the development of an antenna switch, an important RF component is indispensable for these applications. Especially, the switch can be used in both 802.11a and 802.11b systems that employs two antennas for transmit and receive diversity.

The higher operating frequency, 5-6 GHz compared to 1-2 GHz for handsets makes the fabrication of on-chip elements more challenging due to the potential of EM coupling between the elements. Especially, as a DPDT switch, when both antenna 1/antenna 2 to Tx and antenna 2/antenna 1 to Rx are in the on state, the EM coupling between them is inevitable. Therefore, EM simulation is necessary for predicting the RF performance during the circuit design.

Although many GaAs DPDT antenna switch MMICs have previously been reported [1]-[2], those devices cannot be operated with broadband performance from DC through 6GHz while still maintaining low insertion loss, high power handling and high linearity. In this paper, we present a new type of antenna switch IC, which has excellent characteristics of low insertion loss and high power handling capability up to 6 GHz. The device is fabricated using Skyworks's 0.5 micron gate length GaAs pHEMT process.

II. CIRCUIT DESIGN

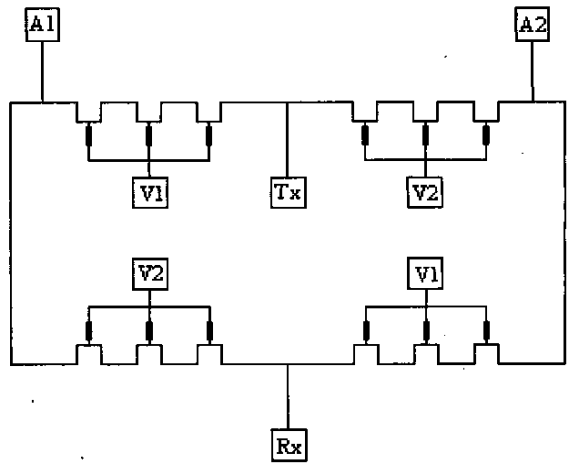

Fig. 1. Schematic circuit of DPDT antenna switch IC

A. Configuration

There are two types of typical configurations to realize DPDT switching function[1]. 1. Back-to-Back structure, Combines both antenna ports of the conventional SPDT switches, which results in a new configuration consisting of two new antenna ports (A1, A2) and the Tx and Rx ports. However the major problem for this structure is higher insertion loss, since the signal has to pass two paths from an antenna to either Tx or Rx. 2. Ring-type structure, combines one RF port of a conventional SPDT switch to another conventional SPDT switch to form a new RF port in a DPDT configuration (Rx port for example). The remaining two RF ports are also combined in a similar fashion (Tx port). We now also have two antenna ports and the Tx and Rx ports as discussed previously. However, The major advantage for this structure is lower insertion loss, because the signal passes through only one path between an antenna and Tx/Rx. This structure, as shown in Fig. 1, is described in this paper.

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B. Topology

After choosing the configuration, we face the topology selection for each path. There are two types of topologies that can be chosen 1. Series-only structure, and 2. Series-shunt structure. Note that we cannot use a conventional series-shunt structure for DPDT switch design; instead, we may consider using a series-shunt-series structure. The potential problem is more insertion loss introduced from inserted shunt FETs. The series combination of FETs presented here significantly improve breakdown voltage. Therefore, increased power handling and decreased Coff due to the function of a capacitive voltage divider. The resulting problem is more insertion loss. However, if the on state resistance for the individual FET is small enough, as is the case for a PHEMT FET, the total resistance for the stacked FET is acceptable.

C. Multi-Gate FETs

A multi-gate approach has successfully been used to improve power handling [3], but a more fundamental problem in switch design for high power and broadband switches is to maintain acceptable insertion loss and isolation. Compared to the single-gate FETs, the multi-gate FET exhibits lower Cds, but higher Ron, bigger Cgsoff and smaller Roff, which is equivalent to increase in Cds. Therefore, the insertion loss of a dual-gate FET is considerably high and even more for a triple-gate FET. Although larger peripheries can be used to maintain a reasonably lower insertion loss at lower frequency, at high frequency, the frequency response rolls off fast due to the increase in Coff. Therefore, insertion loss may not be improved by increasing the peripheries for broadband design.

Next, let us compare the difference of insertion loss and isolation among a single-gate FET, a dual-gate FET and a triple-gate FET. The insertion loss for a single-gate FET is about 0.1 dB lower than a dual-get FET and the insertion loss for a dual-gate FET is about 0.1 dB lower than a triple-gate FET. Although these three structures exhibit acceptable insertion loss, none of them meets isolation requirements. As for two FETs of a single-gate, a dual-gate and a triple-gate, only the single-gate FET shows acceptable insertion loss, and the other two shows greater than 1.1 dB insertion loss. Therefore, a combination of two single-gate FETs in series is a choice. In this design, we choose three FETs in series after considering isolation and large-signal performance. In addition, all four paths are identical, as shown in Fig. 1.

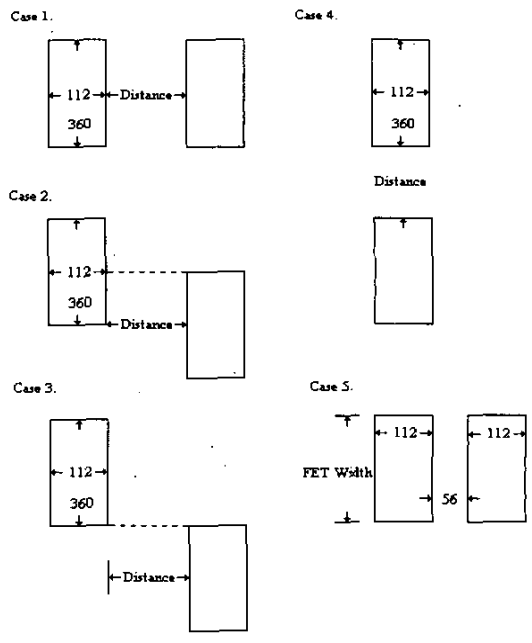

Fig.2. Geometry between two FET sets for various relative positions.

III. EM COUPLING BETWEEN 2 FETs

In order to optimize the switch design at high frequency, we have to use EM simulation tool to predict the circuit performance of each individual component, especially FETs. Using Microwave Office EM simulation tool, we can simplify a FET as a 3-layer structure enclosed by a rectangular box with perfectly conducting walls. The bottom layer is a typical semi-insulating GaAS substrate; the middle one is conductive plating and the top layer is air with thickness much larger than the former two layers. A chain of three single-gate FETs can be simplified as a FET set, a bigger FET, which can be further viewed as a rectangular microstrip patch radiator. When a source patch is excited by a high frequency signal, it radiates EM field to a neighboring patch that produces induced current on its surface to meet the EM boundary conditions. The induced current on the passive patch in turn radiates the EM field back to the first source patch. Thus, mutual coupling exists, which degrades the isolation between two FET sets. Fig. 2 shows the relative positions between two FET sets, and the coupling results at 6 GHz are shown in Fig. 3. The isolation degrades linearly as the distance decreases.

The lowest value is about 20 dB; Case 5 shows the worst isolation because of the strong EM coupling as the patch turns to be bigger. Fig. 4 shows the frequency response of isolation. We can see that the isolation degradation begins around 2.4 GHz at a level lower than 30 dB. Beyond that, the frequency responses are linear too. The reason is obvious, as frequency increases, the electrical size of the FET set also increases. Similar to those in Fig. 3, the isolation decreases.

IV. PERFORMANCE

Measurements have been performed at room temperature on fifty plastic parts. The package is QFN 3*3 mm, 12-lead. The pinouts are as follows: two antenna ports are on the same side of the package, the Tx and Rx ports are on the opposite side, and the two DC controls are on the remaining sides symmetrically. Such pinouts results from the systematic consideration of the radio, but resulting in relatively lower isolation between two antennas and that of Tx and Rx ports, compared with normal path isolation between an antenna and Tx/Rx. These isolation differences can be predicted by EM simulation after considering the mutual coupling between two components. Fig. 5 shows the simulation results. There is about 6 dB difference that may be not explained by a conventional circuit model. Which shows that the isolation between two antennas should be similar to that of an antenna and Tx/Rx, assuming that Ron is small enough. Fig. 6 shows the insertion loss between two normal ports. The typical value of the insertion loss is about 0.8 dB up to 5 GHz. After 5 GHz, the frequency response rolls off quickly due to the larger Coff. The insertion loss is about 0.2 dB lower at 6 GHz compared with that in DC-5 GHz. Fig. 7 shows the isolations between normal paths with minimum of 21 dB. Fig. 8 shows the isolation between antennas and that of Tx and Rx. The measured data is much closer to the EM simulation results shown in Fig. 5. Fig 9 shows the P1dB. We can see that from DC through 5.2 GHz, the power handling is high with P1dB of about 36 dBm with a low control voltage 3V. The power handling degrades slightly at 5.8 GHz. Fig. 10 shows the linearity versus the control voltages. We can see at 3 V or greater, the input IP3 is about 53 dBm up to 5.8 GHz.

IV. CONCLUSION

A broadband and high power DPDT antenna switch IC has been developed. The high performance with low insertion loss and high linearity comes from Skywork's 0.5 micro pHEMT process and its circuit design, implementing EM simulation.

REFERENCES

[1] Kazumasa Kohama, Takahiro Ohgihara, and Yoshkazu Murakami, "High power DPDT Antenna Switch MMIC for Digital Cellular Systems," *IEEE Journal of Solid-State Circuits*. Vol. 31. No. 10, Oct. 1996

[2] Akira Nagayama, Masatoyo Nishibe, Takayuki Inaoka, et al, " Low-Insertion-Loss DP3T MMIC Switch for Dual-Band Cellular Phones," *IEEE Journal of Solid-State Circuits*. Vol. 34. No. 8, Aug. 1999

[3] F.McGrath, C.Varmazis, C. Kermarrec, R.Pratrt, "Novel High Performance SPDT Power Switches Using Multi-Gate FET's," *IEEE MTT-S Digest*, 1991. Pp839-842.

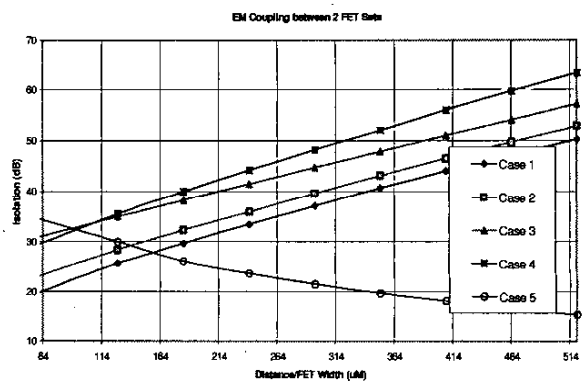

Fig. 3. EM coupling between 2 FET sets for various relative positions.

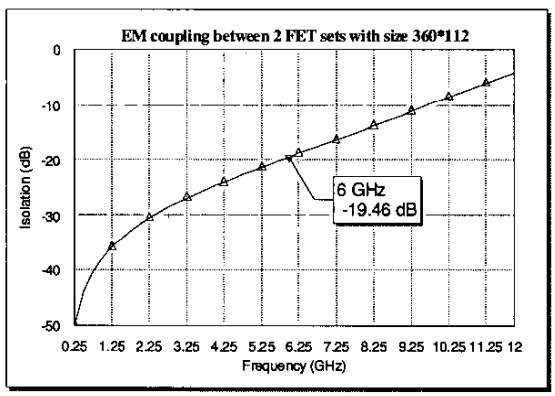

Fig. 4. EM coupling between 2 FET sets versus frequency

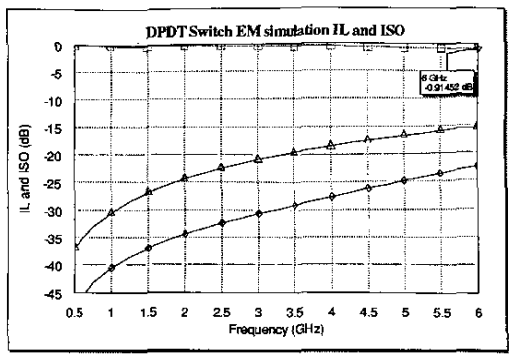

Fig. 5. EM simulation, insertion loss and isolations

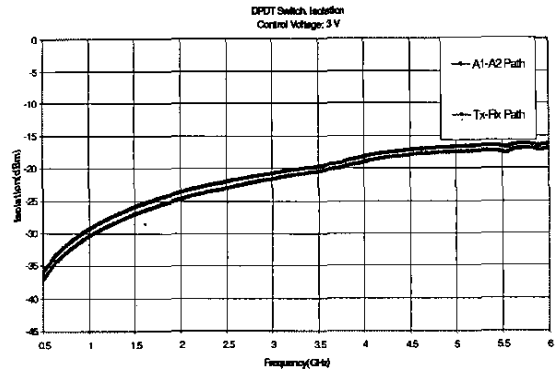

Fig. 8. Isolation between 2 antenna ports/Tx-Rx ports

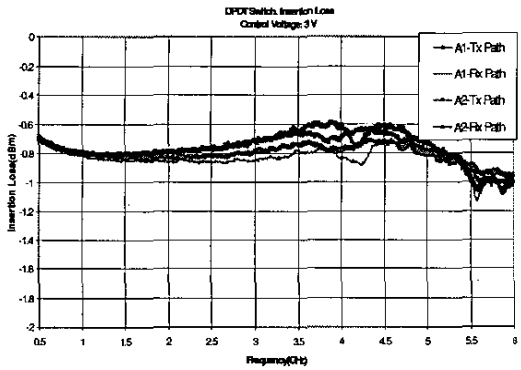

Fig. 6. Insertion Loss between normal operating ports

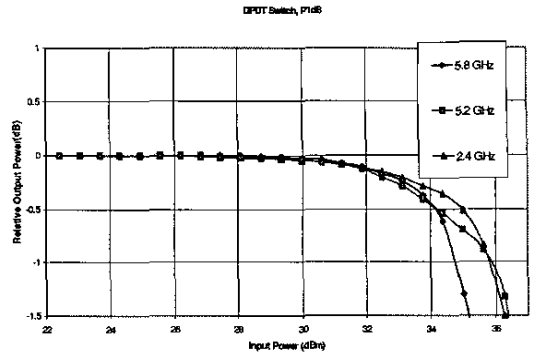

Fig. 9. P1dB for various operating frequencies

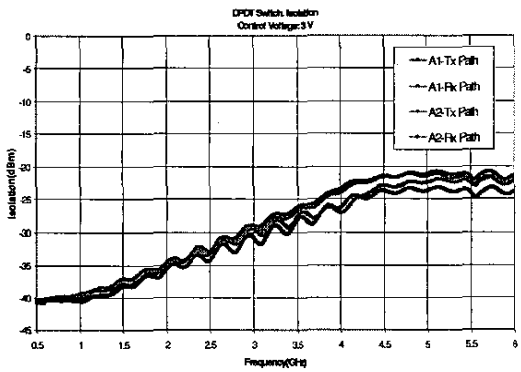

Fig. 7. Isolations between normal operating ports

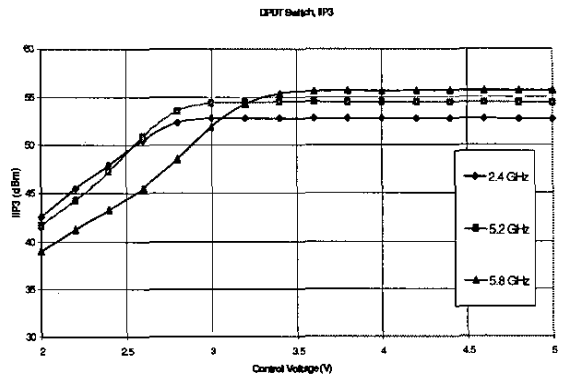

Fig. 10. Input IP3 for various operating frequencies